AMENDMENTS TO THE SPECIFICATION:

Please replace paragraph [0013] with the following amended paragraph:

[0013] To facilitate an understanding of the principles and features of the present invention, it is explained hereinafter with reference to an exemplary embodiment. Figure 1, illustrates an exemplary apparatus for managing the flow of information among plural processors of a processing array depicted as the processor system bus architecture 100 within which the transceiver of the present invention finds utility. This system bus architecture is the subject of copending patent application Serial No. 09/955,961, (Attorney Docket No. 017750-416) filed on even date herewith, entitled "Two Level Multi-Tier System Bus," which is hereby incorporated herein by reference in its entirety. In the processor system bus architecture 100, a system bus 102 is used to interconnect multiple processors. Access to the system bus 102 is controlled by a means for arbitrating access, or the system controller (SC) 104. The system controller 104 contains a Power PC (PPC) processor 106 designated PPC-A and transfers system bus control actions over the system bus 102 using a transfer protocol, described hereinafter with greater detail. The power PC processor 106 is connected to memory 108 and a bus interface device 110, which is connected directly to the system bus 102. Also contained within the system controller 104 is a system bus arbitration unit 112, which is connected directly to the system bus 102 for controlling access to the system bus 102 by various devices connected thereto. This access is arbitrated independently of the processors connected by the system bus 102.